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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,605	09/23/2003	Bernd Karl Appelt	4459-130	9744

7590 06/15/2005

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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/667,605	APPELT ET AL.	
	Examiner	Art Unit	
	Quang D. Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,10-15 and 20-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-15 and 20-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-5, 10-12, 14, 20-22, 24-26 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,266,197 to Glenn et al. in view of US Patent Application Publication No. 2004/0041221 to Boon et al.

Regarding claim 1, Glenn et al. (figures 1-2) teach an optical semiconductor package comprising:

a substrate (102) having opposite upper (the top surface of the substrate [102]) and lower (the bottom surface of the substrate [102]) surfaces;

a chip (sensor chip [106]) having an optical element and disposed on the upper surface (the top surface of the substrate [102]);

a plurality of bonding pads (a plurality of portion of conductive traces [104, 104A]) disposed on the upper surface (the top surface of the substrate [102]);

a plurality of bonding wires (114) electrically connecting the chip (106) to the bonding pads (portions of the conductive traces [104, 104A]);

a window (122) made of a transparent material (column 11, lines 5-10);

a support (a portion of [226]) supporting the window (15) for positioning the window corresponding to the optical element of the chip (106).

Note that a window made of a transparent material for allowing light to transmit through the window and interact with the optical element is a functional language and does not further limit or define the structure and is not given any patentable weight. Additionally, the device taught by Glenn et al. could have been used for the claimed purpose.

Glenn et al. differ from the claimed invention by not showing a transparent encapsulant encapsulating the chip. However, Boon et al. (figure 4) teach a transparent encapsulant (32; column 3, paragraph [0025]) encapsulating the chip (22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Boon et al. into the device taught by Glenn et al. in order to reduce the internal reflection losses of the light. The combined device shows a transparent encapsulant formed on the substrate for fixing the window and encapsulating the chip and the bonding wires.

Regarding claim 2, the claim limitations "the encapsulant is formed by means of an overmolding process" in claim 2 is taken to be product by process limitations, which does not carry weight in claim drawn to structure. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and no the patentability of the

process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding claim 3, the combined device shows matched snapping elements (Glenn et al.; portions of [225I, 225E]) respectively disposed on the window (Glenn et al.; 122) and the support (Glenn et al.; 226) for snapping the window with the support.

Regarding claim 4, the combined device shows the supporter (Glenn et al.; 226) further comprises a shoulder (Glenn et al.; a portion of the recess of [226]) for supporting the window.

Regarding claim 5, the combined device shows the window is a lens (Glenn et al.; layer [122]).

Regarding claim 10, Glenn et al. (figures 1-2) teach an optical semiconductor package comprising:

a substrate (102) having opposite upper (the top surface of the substrate [102]) and lower (the bottom surface of the substrate [102]) surfaces;

a chip (sensor chip [106]) having an optical element and disposed on the upper surface (the top surface of the substrate [102]);

a plurality of bonding pads (a plurality of portion of conductive traces [104, 104A]) disposed on the upper surface (the top surface of the substrate [102]);

a plurality of bonding wires (114) electrically connecting the chip (106) to the bonding pads (portions of the conductive traces [104, 104A]);

a window (122) made of a transparent material (column 11, lines 5-10) mounted on the optical element of the chip (sensor chip [106]).

Note that a window made of a transparent material for allowing light to transmit through the window and interact with the optical element is a functional language and does not further limit or define the structure and is not given any patentable weight. Additionally, the device taught by Glenn et al. could have been used for the claimed purpose.

Glenn et al. differ from the claimed invention by not showing a transparent encapsulant encapsulating the chip. However, Boon et al. (figure 4) teach a transparent encapsulant (32; column 3, paragraph [0025]) encapsulating the chip (22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Boon et al. into the device taught by Glenn et al. in order to reduce the internal reflection losses of the light. The combined device shows a transparent encapsulant formed on the substrate for fixing the window and encapsulating the chip and the bonding wires.

Regarding claim 11, the claim limitations "the encapsulant is formed by means of an overmolding process" in claim 11 is taken to be product by process limitations, which does not carry weight in claim drawn to structure. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and no the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding claim 12, the combined device shows the window comprises a ledge (Glenn et al.; a portion of the recess of [226]) for securing the window in the encapsulant.

Regarding claim 14, the combined device shows the window is a lens (Glenn et al.; layer [122]).

Regarding claim 20, Glenn et al. (figures 1-2) teach an optical semiconductor package comprising:

a substrate (102) having opposite upper (the top surface of the substrate [102]) and lower (the bottom surface of the substrate [102]) surfaces;

a chip (sensor chip [106]) having an optical element and disposed on the upper surface (the top surface of the substrate [102]);

a plurality of bonding pads (a plurality of portion of conductive traces [104, 104A]) disposed on the upper surface (the top surface of the substrate [102]);

a plurality of bonding wires (114) electrically connecting the chip (106) to the bonding pads (portions of the conductive traces [104, 104A]);

a window (122) made of a transparent material (column 11, lines 5-10);

a support (a portion of [226]) supporting the window (15) for positioning the window corresponding to the optical element of the chip (106).

Note that a window made of a transparent material for allowing light to transmit through the window and interact with the optical element is a functional language and does not further limit or define the structure and is not given any patentable weight. Additionally, the device taught by Glenn et al. could have been used for the claimed purpose.

Glenn et al. differ from the claimed invention by not showing a transparent encapsulant encapsulating the chip. However, Boon et al. (figure 4) teach a transparent encapsulant (32; column 3, paragraph [0025]) encapsulating the chip (22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Boon et al. into the device taught by Glenn et al. in order to reduce the internal reflection losses of the light. The combined device shows a transparent encapsulant formed on the substrate for hermetically fixing the support on the substrate.

Regarding claim 21, the claim limitations "the encapsulant is formed by means of an overmolding process" in claim 21 is taken to be product by process limitations, which does not carry weight in claim drawn to structure. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al., 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and no the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding claim 22, the combined device shows the window (Glenn et al.; 122) is hermetically disposed on the support (Glenn et al.; a portion of [226]).

Regarding claim 24, the combined device shows the window is a lens (Glenn et al.; layer [122]).

Regarding claim 25, the combined device shows the optical element comprises an optical sensor (Glenn et al.; sensor chip [106]).

Regarding claim 26, the combined device shows the optical element comprises an optical sensor (Glenn et al.; sensor chip [106]).

Regarding claim 28, the combined device shows the optical element is an optically sensitive element (sensor chip [106]).

3. Claims 13 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. in view of Boon et al., and further in view of US Patent No. 4,732,042 to Adams.

Regarding claims 13 and 23, the disclosures of Glenn et al. and Boon et al. are discussed as applied to claims 10-12 and 14 above.

The combined device differs from the claimed invention by not showing the encapsulant is made of an opaque material. However, Adams teaches the encapsulant (19) is made of an opaque material (column 3, line 40). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Adams into the device taught by Glenn et al. and Boon et al. in order to protect light sensitive circuit of the device.

4. Claims 15 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Glenn et al. in view of Boon et al., and further in view of US Patent No. 5,897,338 to Kaldenberg.

The disclosures of Glenn et al. and Boon et al. are discussed as applied to claims 10-12, 14 and 26 above.

Regarding claim 15, the combined device differs from the claimed invention by not showing an adhesive for mounting the window on the optical element of the chip. However, Kaldenberg (figure 4) teaches an adhesive (28) for mounting the window (26) on the chip (12). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kaldenberg into the device taught by Glenn et al. and Boon et al. in order to hold the window in place.

Regarding claim 27, the combined device shows the window (Glenn et al.; 122) has opposite upper (top surface) and lower (bottom surface) surfaces and a side surface (Glenn et al.; 122S) connecting the upper (the top surface) and lower (bottom surface) surfaces of the window (Glenn et al.; 122).

The combined device differs from the claimed invention by not showing the package further comprises a transparent adhesive layer attaching the lower surface of the window to an upper surface of the optical element of the chip; and the encapsulant surrounds the window and directly contacts the side surface of the windows, while leaving the upper surface of the windows exposed from an upper surface of the encapsulant. However, Kaldenberg (figures 1-4) teaches an adhesive layer (28) attaching the lower surface of the window (the portion of opening [20]) to an upper surface of the optical element of the chip (12); and the encapsulant (a portion of [24]) surrounds the window (a portion of [20]) and directly contacts the side surface of the windows (20), while leaving the upper surface of the windows (20) exposed from an upper surface of the encapsulant (24). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Kaldenberg into the device taught by Glenn et al. and Boon et al. in order to protect the window and the chip.

5. Claims 29 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,838,089 to Okada et al. in view of US Patent No. 6,266,197 to Glenn et al.

Regarding claim 29, Okada et al. (figures 1-2) teach an optical semiconductor package, comprising:

a substrate (12) having opposite upper (top surface of substrate [12]) and lower (bottom surface of substrate [12]) surfaces;

a chip (18) disposed on the upper surface (top surface of substrate [12]) of the substrate (12) and having an optical sensor (sensor chip [18]);

a plurality of bonding wires (24) electrically connecting the chip (18) to the substrate (12);

a supporting wall (28) extending upwardly from the upper surface (the top surface of substrate [12]) of the substrate (12);

a window (a portion of [32]) supported by the supporting wall (28) at a location above the optical sensor (sensor chip [18]); and

an encapsulant (36) formed on the upper surface of the substrate (12) to surround the supporting wall (28).

Note that a window made of a transparent material for allowing light to transmit through the window and interact with the optical element is a functional language and does not further limit or define the structure and is not given any patentable weight. Additionally, the device taught by Okada et al. could have been used for the claimed purpose.

Okada et al. differ from the claimed invention by not showing a window made of a transparent material. However, Glenn et al. (figure 2) teach a window (122) made of a

transparent material (column 11, lines 5-10). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Glenn et al. into the device taught by Okada et al. in order to improve the light-passing performance.

Regarding claim 31, the combined device shows the encapsulant (Okada et al.; 36), the supporting wall (Okada et al.; 28), the window (Okada et al.; the portion of [32]) and the substrate (Okada et al.; 12) together define a hermetically sealed cavity in which the chip (Okada et al.; 18), the optical sensor and the wires (Okada et al.; 24) are disposed.

6. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okada et al. in view of Glenn et al., and further in view of US Patent Application Publication No. 2004/0041221 to Boon et al.

Regarding claim 30, the disclosures of Okada et al. and Glenn et al. are discussed as applied to claim 29 above.

The combined device shows the encapsulant includes an outer portion (Okada et al.; a portion of encapsulant [36]) covering an outer side surface of the supporting wall (Okada et al.; 28).

The combined device differs from the claimed invention by not showing a transparent encapsulant encapsulating the chip. However, Boon et al. (figure 4) teach a transparent encapsulant (32; column 3, paragraph [0025]) encapsulating the chip (22). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Boon et al. into the device taught by Okada et al. and Glenn et al. in

order to reduce the internal reflection losses of the light. The combined device shows an inner portion encapsulating the chip and the wires and covering an inner side surface of the supporting wall, wherein the inner portion of the encapsulant is transparent.

Response to Arguments

Applicant's arguments with respect to claims 1-5, 10-15 and 20-31 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D. Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
June 6 2005

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